1. Name two areas of application of FPGAs.
   * Consumer Automotive, and Communications Broadcast
2. What was the main goal for basic TTL digital logic design and what were the main challenges?
   * The Main Goal of TTL digital logic is to create designs with few chips as possible to reduce cost and minimize Circuit Board real estate. The Main challenge to TTL logic design is the complication that arise from implement the design output with few chips this can lead to too many wiring between chips or too many routing on the printed circuit board.
3. What are the steps for designing basic Digital logic Designs?
   * Step 1 design a Truth table with all inputs and possible outputs [Output = 2n x m] where n=inputs and m=bits for each output
   * Step 2 create a Karnaugh map (K-map), this will be used to make the minterm which can be used to form the logic equation of the design at that stage.
   * Step 3 choose the types of logic chips (AND, NAND, OR, XOR etc.) to implement the TTL design logic.
   * Step 3 Cascade different logic when necessary if a selected logic chip is not available or costly.
   * Step 4 Perform a Design Rule Check (DRC) and Electrical Rule Check (ERC) of the final design base end user’s application of the design.
   * Wire the Desing together or implement on a PCB.
4. How is combinatorial logic implemented?
   * Combinational logic can be implemented using Programmable Logic Arrays (PAL), PLD, FPGA, etc.
5. How is data synchronized and stored in logic circuits?
   * Data can be synchronized and store in logic circuits using Registers.
6. What were the main ideas that led to the creation of programmable devices?
   * To have fixed logic functions combined into a single device, where the routing can be controlled or programmed.
7. What are the main sections of a PAL? State briefly what each section contains.
   * Programmable array: this is where the desired inputs are selected and routed to the AND gate.
   * Product Terms: Forms the Output of the AND gate to form the product function.
   * Macrocell: this is where the Memory or synchronization occurs the out of the AND gates are connected to an OR gate.
8. What are some of the advantages of PALs?
   * Fewer devices required.
   * Less Board (real estate)
   * Lower cost
   * Power savings
9. What is the key technology used to control the interconnection fabric in the early PAL Devices? Where is this technology still used?
   * Floating Gate Transistors are the key technology used in early PAL devices.
   * This technology is still used in Flash Memory Technology
10. What was the first version of PLDs called? What were the main differences between the PLDs and the PAL Devices?
    * The 22V10 was the first version of PLDs.
    * The main difference between PLDs and PALs are the inclusion of Variable Product Term Distribution and Fully Programmable MacroCells.
11. What was the innovation in CPLDs?
    * The main innovation in CPLDs is the I/O (control & pins) and Programmable Interconnect.
12. What are LABs? How different is it from a PAL?
    * LABS are Logic Array Blocks, that contain multiple macrocells, local programmable interconnect like PLD, and Expander product term logic.
    * The main different between LABs and PLDs is that LABs have Expander Product Terms
13. What are the advantages and disadvantages of expander product terms?
    * Provides controlled product-term distribution and expansion which can be shared with other macrocells, so a product term needs to be created only once.
    * The expander product term introduces an extra delay.
14. What does JTAG stand for and what is it used for?
    * JTAG stands for Joint Test Action Group
    * JTAG provides a standard and port to test, program, and Debug CPLDs, FPGAs, and other ICs without the need for probing, it can also be used to test PCBs without probing every test point on the PCB.
15. What are the major additions to the FPGAs if compared to CPLDs?
    * FPGAs add an on chip nonvolatile configuration memory Blocks, DSP Blocks, PLLs, Transceivers, Hardened IP Blocks, etc.
16. As a summary, sketch a block diagram showing the distinct phases of evolution of programmable devices with the major additions for every stage.

**FPGA**

I/O (control & pins)

Logic Array Block (LABs)

Expander Product Terms

Programmable Interconnect Arrays (PI)

Programmable Interconnect

In-System Programming (ISP) with JTAG

Memory Blocks

DSP Blocks

PPLs

Transceivers

Hardened IP Blocks

**PLD**

Programmable Array

Variable Product term Distribution

Programmable Macrocell

**CPLD**

I/O (control & pins)

Logic Array Block (LABs)

Expander Product Terms

Programmable Interconnect Arrays (PI)

Programmable Interconnect

In-System Programming (ISP) with JTAG

**PAL**

Programmable Array

Product terms

Macrocell